Charge Pump Design

Additional Slides

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Introduction

- Charge pumps are widely used to generate voltages beyond normal supply range
  - high voltages for programming and erasing of floating gate in EEPROMs and Flash memories
  - negative voltages for substrate bias for reducing leakage in certain digital designs

- Typically generate 16-18V from 1.8V supply for program and erase in a Flash memory
  - have multiple program voltages in multi-level cell (MLC) Flash memory

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- Cascade more number of stages
- Two-phase clock used for charge transfer during both the phases
Dickson Charge Pump

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Dickson Charge Pump Operation

- Assume, small capacitive load and negligible parasitics. Neglect body effect.

\[ V_{out} = N(V_{DD} - V_{THN}) \]
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Four-phase Charge Pump

- Bootstrap the gates of the charge transfer devices \((M_1, M_3, \ldots)\) to avoid the \(V_{THN}\) drop

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Precharge the gate of the charge transfer device $M_1$ (i.e. node $n_a$) in one half-cycle and discharge in the other half.

- $C_{b1}$ is the boosting capacitor.
- Boost the node $n_a$ by $V_{DD}$ in the charge transfer phase ($\phi_2$ is high).
- Full charge is passed from $n_1$ to $n_2$.
- $V_{THN}$ drop is cancelled!
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Four-phase Charge Pump

- Overlap between $\phi_1$ and $\phi_3$ by roughly 10% of $T_{CK}$
  - Precharge gate of the transfer device to its drain potential before bootstrapping occurs
  - Prevent backward leakage of charge
- $\phi_2$ and $\phi_4$ are used to boost the potential of nodes $n_a$ and $n_b$ resp.
  - $\phi_2$ shouldn’t overlap with $\phi_3$ in high phase
  - $\phi_4$ shouldn’t overlap with $\phi_1$ in high phase
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Basic Concept Dickson Charge Pump 4-phase Charge Pump Non-overlapping Clocks Voltage Regulation

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Assume steady-state conditions

- $\phi_1$ goes high $\rightarrow$ $n_a$ is precharged to $2V_{DD} - V_{THN}$
- $\phi_3$ goes low $\rightarrow$ $M_2$ is off
- $\phi_2$ goes high $\rightarrow$ $n_a$ is bootstrapped to $3V_{DD} - V_{THN}$
  - full charge is transferred through $M_1$
- $\phi_3$ goes high $\rightarrow$ $n_b$ is precharged to $3V_{DD} - V_{THN}$
- $\phi_1$ goes low $\rightarrow$ $M_4$ is off
- $\phi_4$ goes high $\rightarrow$ $n_b$ is bootstrapped to $4V_{DD} - V_{THN}$
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Other Architectures: Controllable Body Voltage

- Adjust bulk voltage to get rid of the body effect [3].
- Better than Dickson CP, but $V_{THN0}$ drop still exists.
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- Better than Dickson CP, but $V_{THN0}$ drop still exists.
Non-Overlapping Clocks

\[ \text{CK} \quad ? \quad \phi_1 \quad \phi_2 \quad \text{CK} \quad \phi_1 \quad \phi_2 \]
Non-Overlapping Clocks
Non-Overlapping Clocks: State Machine

**State Diagram**

- States: 01, 00, 10
- Transitions:
  - From 01 to 00: CK = 1, φ1 = 0, φ2 = 0
  - From 00 to 10: CK = 1, φ1 = 1, φ2 = 1
  - From 00 to 00: CK = 1, φ1 = 1, φ2 = 0

**Truth Table**

<table>
<thead>
<tr>
<th>CK</th>
<th>φ1</th>
<th>φ2</th>
<th>φ′1</th>
<th>φ′2</th>
</tr>
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<tbody>
<tr>
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<td>1</td>
</tr>
</tbody>
</table>
Non-Overlapping Clocks: Karnaugh Maps

\[
\begin{array}{c|ccccc}
\text{CK}/\phi_1 \phi_2 & 00 & 01 & 11 & 10 \\
\hline
0 & 0 & 0 & X & 0 \\
1 & 1 & 0 & X & 1 \\
\end{array}
\]

\[
\phi'_1 = CK \cdot \overline{\phi_2} = \overline{CK} \cdot \phi_2
\]

\[
\begin{array}{c|ccccc}
\text{CK}/\phi_1 \phi_2 & 00 & 01 & 11 & 10 \\
\hline
0 & 0 & 1 & 1 & X & 0 \\
1 & 0 & 0 & X & 0 \\
\end{array}
\]

\[
\phi'_2 = \overline{CK} \cdot \overline{\phi_1} = \overline{CK} \cdot \phi_1
\]
Non-Overlapping Clocks: Generation Circuit 1

- Implements logic $\phi_1' = CK \cdot \overline{\phi_2}$ and $\phi_2' = \overline{CK} \cdot \overline{\phi_1}$
- Non-overlap time is set by the NAND’s $t_{pLH}$
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- Non-overlap time is set by the NAND’s $t_{PLH}$
Can increase non-overlap time by inserting extra delay
- Insert a matched delay to the inverter for perfect timing.
Another topology with larger non-overlap time.
The following circuit generates four non-overlapping clock phases.

The phase alignment for 4-phase charge pump is slightly different. Think about it!

**Figure 2.38** Generating a four-phase non-overlapping clock signal.
The following circuit generates four non-overlapping clock phases.

![Circuit Diagram]

**Figure 2.38** Generating a four-phase non-overlapping clock signal.

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Regulated Charge Pump

- Feedback to regulate the charge pump output to a desired voltage
- A sensing circuit compares the pump output to a reference and enables the clock
- A simple method is to switch the ring oscillator on and off
- Large ripples in the output
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- Cap values $C_1$ and $C_2$ change with parasitics.
- Capacitive loading on the pump (may be insignificant w.r.t. $C_L$)
- Faster feedback control.

![Diagram of Capacitive divider feedback control](image)

Figure 4-19 Capacitive divider feedback control.
- Cap values $C_1$ and $C_2$ change with parasitics.
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**Figure 4-19** Capacitive divider feedback control.
Pump Regulation: Capacitor Divider

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![Diagram of Capacitive Divider Feedback Control]

**Figure 4-19** Capacitive divider feedback control.
Resistors may load the pump output.

- Use large resistors → Large layout area
- RC delay

![Diagagram](Image)
Resistors may load the pump output.

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Figure 4-20: Resistive divider feedback control.
Resistors may load the pump output.

- Use large resistors → Large layout area

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Figure 4-20: Resistive divider feedback control.
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Figure 4-20  Resistive divider feedback control.
- Resistors may load the pump output.
- Use large resistors $\rightarrow$ Large layout area

![Resistive divider feedback control diagram](Figure 4-20)
Use a NAND gate in the ring, while ensuring there are odd number of inverting stages
Use a voltage-controlled oscillator (VCO) for smoother regulation of the output[5].

- cleaner VCO switching leads to much lower pump output ripples.
VCO based Regulation

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  - cleaner VCO switching leads to much lower pump output ripples.
Automatically tune the buffer strength to regulate the output[5].
References I


