Cascade of Integrators with feed-forward summation (CIFF)

- Use feedforward paths rather than feedback ones to create the zeros of the NTF.

By inspection:

1. \( I(z) = \frac{1}{z-1} = \frac{z}{z-1} \) - delaying integrator/accumulator.
2. \( L_1(z) = -a_1I(z) - a_1I^2(z) - \ldots - a_nI^n(z) \)
3. \( L_0(z) = b_1(a_1I + a_1I^2 + \ldots + a_nI^n) + b_2(a_2I + \ldots + a_nI^{n-1}) + \ldots + b_{n+1} \)

\[ L_1(z) = -\frac{a_1 + a_1(z-1) + \ldots + a_n(z-1)^{n-1}}{(z-1)^n} \quad \text{Same as in CIFB} \]
\[ L_0(z) = \frac{\gamma_1 + \gamma_2(z-1) + \ldots + \gamma_n(z-1)^{n-1} + \gamma_{n+1}(z-1)^n}{(z-1)^n} \]

\( \gamma_{n+1} = b_{n+1} \)
\( \gamma_n = b_1 a_1 + b_2 a_2 + b_3 a_3 + \ldots \)
\( \gamma_{n-1} = b_1 a_n + b_2 a_n + b_3 a_n + \ldots \)
\( \gamma_1 = b_1 a_n \)

\( \mathcal{L} \) is the generic case is not used in the Toolbox.
Now, consider the case when $b_2 = b_3 = \ldots = b_n = 0$ and $b_1 = b_{n+1} = 1$.

\[ L_0(z) = \frac{1}{1-z_1} - \frac{1}{1-z_1} = \frac{1}{1-z} \quad \text{when } b_{n+1} = 1 \]

\[ L_0(z) = 0 \quad \text{when } b_{n+1} = 0. \]

From (1), we have when $b_{n+1} = 1$ (full input feedforward case)

\[ \text{STF}(z) = \frac{L_0(z)}{1-L_1(z)} = 1, \quad \text{Also } \quad \text{NTF}(z) = \frac{1}{1-L_1(z)} \]

when $b_{n+1} = 0$, (only input is coupled)

\[ \text{STF}(z) = 1 - \text{NTF}(z) = \frac{L_1(z)}{1-L_1(z)}, \quad \text{NTF}(z) = \frac{1}{1-L_1(z)} \]
when \( b_1 = b_{n+1} = 1 \)

\[
\text{STF} = 1
\]

\[
\Rightarrow \quad U(z) - V(z) = U(z) - \frac{[U(z) + NTF(z)E(z)]}{V(z)} = \frac{NTF(z)E(z)}{V(z)}
\]

\[\Rightarrow \text{Loof filter doesn't process the input signal U(z) at all.}\]

\( \text{Lo low distortion case} \)

\( \text{Lo same results apply to relaxed integrator implementation as seen for the CIFB low-distortion case.} \)

\[
\text{Note that implementing the low-distortion condition is easier with CIFF (only 2 branches) as opposed to (n+1) input coupling branches required for the CIFB case.}
\]

\[
\text{When } b_{n+1} = 0 \Rightarrow \text{only input coupling is used then we saw that}
\]

\[
\text{STF(z)} = 1 - \text{NTF(z)}
\]

\[\Rightarrow \text{results in high-frequency peaking in the STF.}\]

\( \text{Lo add pre-filter to the input in this range to avoid overloading in the modulator.} \)

\( \text{or modify the NTF/STF} \)

\( \text{Lo can use other b's to alleviate the noise peaking.} \)

\( \text{Lo figure this out for CIFF/CIFB topologies.} \)
- Add resonator feedbacks to create complex NTF given to CRFF (Cascade of Resonators with feed-forward summation).

- Can also use double-delaying resonators to modify the CRFF topology.

- Same analysis for resonators as seen for the CRFB/CFBF cases.

- Here, multiple input feed-in branches are also possible. Using $f(2, n)$.

  To modify toolbox function?
Comparison between FB and FF topologies:

**Feed Forward**
1. FF has relaxed dynamic range requirements.
2. If full-FF is not used (but, 20)
   STF peaking occurs.
   Leads to a problem in LT-DSMs
3. Only one DAC required
4. Needs a summation block
5. Timing can be tricky.
   Need to quantize it and feed it back in zero time.
6. First integrator is fastest
7. First opamp is power hungry
   (noise reasons)
8. → Best optimization for opamp power consumption
9. Small capacitor area

**Feed Back**
1. Integrator outputs contain significant amount of input signal as well as
   filtered quantization noise (Typically)
2. STF has good attenuation beyond the signal band
   → Better AAF in LT-DSMs.
3. Requires many feedback DACs.
4. No extra summer required.
   Not an issue
5. Last integrator is fastest
   (has large signal content)
6. First opamp is power hungry
   (noise reasons)
7. → First and last opamps are
   power hungry, more power is burnt.
8. Large capacitor area to accommodate the
   large signal swings
   → DRS results in large C’s.
   → More power burnt in opamps
   → Larger layout size.

If STF/AAF is not an issue, CIF architecture is generally preferred.
Consider a DC input to the CFB modulator with $b_i=0$ for $i>1$, and 1-bit quantizer feedback.

Each integrator has a DC gain. If the sum of all inputs is 0, the integrator output will remain constant, preventing any DC component from appearing at the integrator input. Otherwise, the loop filter will saturate.

One input is the 1-bit feedback path, and the other is the output of the previous integrator, i.e., $(X_{i-1})$.

$Xi_i$ must have a DC component to counteract the DC component of the 1-bit feedback.

Each integrator output contains a combination of filtered quantization noise and a low-frequency component equal to the input signal.

From simulation, the signal component in $Xi$ is significantly larger than the noise component. To allow larger integrator swings, we must ensure $(max(X_i) > max(X_{i-1}))$ (verify this for yourself).

To meet the required integrator feedback caps to limit the swing, we need larger integrator feedback caps. This results in a dynamic range scaling (DRS) that requires larger $C_f$ values.

CFB circuits tend to be larger and more power hungry than the FF ones.
Multi-stage Modulators

- For low-ASK values, it's no longer possible to obtain high SNR values in a single (quantizer) loop modulator by raising the order of the loop-filter.
  
  \[ L \rightarrow \text{MAX} \uparrow \quad \text{as ORDER} \uparrow \]
  
  \[ L_0 \text{ can increase quantizer resolution} \]
  
  \[ L_0 \text{ Flash ADC design becomes complicated} \]
  
  \[ L_0 \text{ DAC\, lin. issues (complex 2^N DEM for large \text{NLZ})} \]
  
  \[ L_0 \text{ complexity } \# \text{as } 2^n \]
  
  \[ \text{max } 4-5 \text{ bits quantizer is employed.} \]

- Use digital cancellation of noise, rather than filtering, by using a multistage (cascade) structure of the modulator.

1. L-0 cascade (Leslie-Singh Structure).

- 1st-order AS modulator in the first stage, followed by a
  static (zero-order) DCC in the second stage, e.g., a 4-bit DCC of resolution.

- Combine the outputs of the two stages, \( V_1 \) & \( V_2 \) to obtain the overall top output \( V \).
Let $e_{1[n]}$ be extracted in analog form by

$$e_1 = v_i - y_1$$

$\Rightarrow$ $e_1$ is then converted to digital form by a multi-bit ADC forming the 2$^{nd}$-stage.

- ADC introduces a second-quantization noise $e_{2[n]}$.
  - $|e_{2[n]}| << |e_{1[n]}|$
  - 2$^{nd}$-stage can have arbitrary latency (no feedback loop around it)

A realized using a low complexity pipelined ADC.

- $v_i$ and $v_i$ are filtered by digital stages, $H_1$ and $H_2$ respectively, and then "added" together.

$\Rightarrow H_1(z) = z^{-k}$ simply matches the latency of the 2$^{nd}$-stage.

$\Rightarrow H_2(z)$ is digital equivalent of the first-stage NTF.

$\Rightarrow V(z) = H_1(z) \cdot V_i(z) - H_2(z) \cdot V_i(z)$

$$\Rightarrow z^{-k} \left[ \text{STF}_1 \cdot U + \text{NTF}_1 \cdot E_1 \right] - \text{NTF}_1 \cdot z^{-k} \cdot \left[ E_1 + E_2 \right]$$

$$= z^{-k} \left[ \text{STF}_1 \cdot U - \text{NTF}_1 \cdot E_2 \right]$$

if $E_1$ is perfectly cancelled, i.e. $H_2 = \text{NTF}_1$

- Compare $V(z)$ with $V_i(z)$:

  Except for the delay of $z^{-k}$,
  - $E_1(z)$ is replaced by $-E_2(z)$
  - P.S.D. level $E_2(z)$ is much smaller than that of $E_1(z)$

  It's cheaper to construct a pipelined ADC than a multi-bit-loop quantizer.

  Lo enhances SSB by as much as 25-30 dB.
*To obtain $e[n]$ by subtracting the quantization of the quantizer must be delay-free, which may not be practical.

$$e[n] = V[n] - y[n]$$

not possible with finite quantizer delay

\[ \text{delay} \rightarrow y[n] \text{ must be delayed before subtraction can be carried out} \]

by doing using switched-cap techniques.

* To avoid the subtraction altogether, the input signal of the second stage can be chosen as $y[n]$, instead of $e[n]$.

Then, we have

$$V_1(z) = V(z) - E_1(z) = STF_1 \cdot U + (NTF_1-1)E_1$$

keeping $H_1(z) = z^k$, but choosing $H_2$ as

$$H_2(z) = \frac{NTF_1(z)}{NTF_1(z)-1}$$

the overall output has become

$$V(z) = z^k \frac{STF_1 \cdot U + NTF_1 \cdot E_1}{NTF_1(z)-1} - \frac{NTF_1(z)}{NTF_1(z)-1} \cdot z^k \frac{STF_1 \cdot U + (NTF_1-1)E_1 + E_2(z)}$$

* Assuming ideal cancellation of terms, we get

$$V(z) = \frac{z^k \cdot STF_1(z)}{1 - NTF_1(z)} \cdot U(z) + \frac{z^k \cdot NTF_1(z)}{1 - NTF_1(z)} \cdot E_1(z)$$

\[ \text{in the signal band} \quad |NTF(z)| < 1 \] then

$$\frac{NTF_1(z)}{1-NTF_1(z)} \leq NTF_1 \text{ in the signal band}$$

one can get SQNR close to the value one obtained earlier.
Disadvantage:

- $Y(z)$ contains $U(z)$ as well as $E(z)$
- $L_0$ second-stage must be able to handle a larger input signal.
- Also the second-stage must have lower distortion in processing the $U(z)$ input.
- $L_0$ not very attractive overall.

Consider one of the low-distortion structures:

- E.g., CIFB with $b_i=a_i$ and $b_{NH} = 1$,
- or CIFF with $b_i=b_{NH} = 1$ and $b(z) = 0$

In both cases have $STF = 1$.

$L_0$ output of the last integrator in the cascade is:

$$X_u(z) = Y(z) - B_w U(z)$$

$$= STF(z) U(z) - (1 - NTF(z)) E(z) - B_w U(z)$$

$$= X_u(z) = -(1 - NTF(z)) E(z)$$

This signal $X_u(z)$ can be used as the input for the second-stage of the $L_0$ cascade.

$L_0$ doesn't contain any $U(z)$.

$L_0$ second-stage need not very linear.

Example topology:

- 2nd order CIFF

![Diagram](image)

$N_{TF} = (1 - z^{-1})^2$

$STF = 1$

$x = -z^{-2} E_1(z)$

$L_0$ feed directly to the second-stage input.
ECE 697 Delta-Sigma Converters Design

Lecture#16 Slides

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CIFF Example 1

- CIFF, order = 4
- All NTF zeros at z=1, i.e. opt = 0.
- Low-distortion topology
  - b(1) = b(5) = 1
  - b(2:4) = 0
- a = [2.1 1.9 0.86 0.16]
- b = [1 0 0 0 1]
- c = [1 1 1 1]
- g = [0 0]

File: CIFB_4th_Order_1.m

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CIFF Example 1 contd. : NTF and STF

File: CIFF_4th_Order_1.m

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CIFF Example 1 contd. : Loop-Filter States

File: CIFF_4th_Order_1.m

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CIFF Example 1 contd.: Simulated Spectrum

$\text{SNDR} = 80.4 \text{ dB}$

$\text{ENOB} = 13.06 \text{ bits}$

@ $\text{OSR} = 16$

File: CIFF$_{4}^{\text{th}}$ Order 1.m

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CIFF Example 2

- CIFF, order = 4
- All NTF zeros at $z=1$, i.e. opt = 0.
- Only single input feed-in used
  - $b(2:end)=0$
- $a = [2.1 \ 1.9 \ 0.86 \ 0.16]$
- $b = [1 \ 0 \ 0 \ 0 \ 0]$
- $c = [1 \ 1 \ 1 \ 1]$
- $g = [0 \ 0]$

File: CIFB_4th_Order_2.m

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CIFF Example 2 contd. : NTF and STF

- Notice the significant STF peaking!

File: CIFF_4th_Order_2.m

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Last integrator output has significant signal content

- Use dynamic range scaling.
- Last integrator will burn more power in this case.

File: CIFF_4th_Order_2.m
CIFF Example 2 contd.: Simulated Spectrum

Modulator Output Spectrum

SNDR = 82.1 dB  
ENOB = 13.34 bits  
@OSR = 16

File: CIFF_4th_Order_2.m  
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Other Examples of Feed-forward Topologies

- Low-distortion CRFF topology
  - CRFF_4^{th}\_Order\_1.m
- CRFF with single feed-in
  - CRFF_4^{th}\_Order\_2.m
- Low-distortion CIFF topology with optimized NTF zeros
  - CIFF\_Opt_4^{th}\_Order\_1.m
- CIFF with single feed-in and optimized NTF zeros
  - CIFF\_Opt_4^{th}\_Order\_2.m
- STF peaking in FF topologies with single feed-in is an issue
  - CT FF DSM will have STF peaking as full-feedforward branch can’t be used.
  - The feed-in coefficients b’s can be strategically used to realize CIFF/CRFB topology with better out-of-band STF attenuation.
L-0 Cascade Simulation

- TBD

File: TBD.m  © Vishal Saxena