Loop Stability Analysis

*Differential Opamp Simulation*

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The STB analysis linearizes the circuit about the DC operating point and computes the loop-gain, gain and phase margins (if the sweep variable is frequency), for a feedback loop or a gain device [1].


Uses return ratio analysis method to calculate loop-gain and phase margin ([3, 4]).
Example Single-ended Opamp Schematic
Pay attention to the **iprobe** component (from analogLib)
- Acts as a short for DC, but breaks the loop in stb analysis
- Place the probe at a point where it **completely breaks (all) the loops.**
• Annotating the node voltages and DC operating points of the devices helps debug the design

• Check device gds to see if its in triode or saturation regions

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Simulation Setup

- Always have dc analysis on for debugging purpose
Bode Plot Setup

- Results → Direct Plot → Main Form
Loop Response Bode Plots

- Here, \( f_{un} = 152.5 \text{ MHz} \), PM=41.8\(^\circ\)

- Try to use the stb analysis while the circuit is in the desired feedback configuration
  - Break the loop with realistic DC operating points
Transient Step Response Test Bench

- Transient step-response verifies the closed-loop stability
- Use small as well as large steps for characterization
- iprobe acts as a short (can remove it from transient sims)
Small Step Response

- Observe the ringing (PM was 41º)
  - Compensate more!
  - Correlate small-step response with the open-loop frequency response for your understanding.
Use large steps for large signal response

- Not captured by the small-signal analysis
- Note the slewing in the output here
Fully-Differential Opamp Simulation

Continuous-time CMFB
CMDM Probe

- Located in library: AnalogLib→cmdmprobe
- Variable CMDM =
  - -1 measures differential mode response
  - +1 measures common mode response
- In IC615, diffstbprobe is available which handles unbalanced differential circuits better than the cmdmprobe.
- More information on the differential probes and the STB analysis algorithm can be found in [4].
Fully Differential Circuit Analysis

- Use CMDM probe for differential analysis [1, 3]
- Placement of the CMDM probe should break the differential as well as the common-mode loops.
For internal loops, isolate those loops individually and perform STB analysis

- Ensure overall DC feedback for accurate biasing and that all loops are compensated
- CMDM$_1$ measures only the first-stage CM response
- CMDM$_2$ measures overall DM response and second-stage CM response
cmdmprobes placed outside DM loop, only in CMFB loops
- CMDM₁ measures only the first-stage CM response
- CMDM₂ measures only the second-stage CM response
- But need another CMDM probe to measure DM loop stability
- Results match with iprobe results very well.
Fully Differential Opamp Schematic

- Two-stage fully differential opamp
- Class AB output stage for large voltage swing
- With individual CMFB.
- 1st stage CMFB compensated
Be noted that the nulling resistors should be connected before the inputs of cmdmprobe in the 1st CMFB loop, or it will generate incorrect results.
- Need one extra cmdmprobe to measure DM loop comparing to method 1.
DM Loop Bode Plots M1&M2

- Differential Mode loop gain and phase margin plots
- Same results obtained by using Method 1 and Method 2

Phase margin = 65.1422 Deg at frequency = 36.1282 MHz.
1st Stage CMFB Loop Bode Plots

Method 1

Phase margin = 64.5059 Deg at frequency = 21.2729 MHz.

Method 2

Phase margin = 64.5788 Deg at frequency = 21.2722 MHz.
2\textsuperscript{nd} Stage CMFB Loop Bode Plots

Method 1

Phase margin = 42.6336 Deg at frequency = 119.604 MHz.

Method 2

Phase margin = 42.376 Deg at frequency = 119.867 MHz.
Simulation Setup

- Use previous oppt (operating point) in the stb analysis
Bode Plot Setup

- Results → Direct Plot → Main Form
DM Transient

- Unity-gain inverting amplifier transient response with a 200mV differential step (rise/fall time=0.1ns, pulse width=100ns)
Unity-gain inverting amplifier transient response with a 100mV common mode step (rise/fall time=0.1ns, pulse width=100ns)
Fully-Differential Opamp Simulation

Switched-capacitor CMFB
Switched Capacitor CMFB Simulation

- 2-stage Class AB output Opamp
- Individual SC-CMFB
PSTB Analysis Using Method 1

- PSTB analysis is essential for sampled circuit
- We can only set the number of harmonics to 0 by choosing Shooting method
- tstab parameter can be obtained by tran analysis first
Go to Simulation → Options → Analog → Main in the ADE window to setup tolerance options accordingly. If the frequency of periodic small signal analyses followed by PSS is high (e.g. 1G), the maxacfreq parameter (options → accuracy) of the PSS can be used to specify the highest frequency, otherwise, the frequency analysis in PAC maybe truncated.
Results → Direct Plot → Main Form

- X-axis scale range is 1/sampling clock frequency
PSTB is always followed by PSS
Results → Direct Plot → Main Form
DM Loop Bode Plots

- **Resistive feedback**
  - Phase margin = 67.0107 Deg at frequency = 48.633 MHz.

- **Capacitive feedback**
  - Phase margin = 64.0631 Deg at frequency = 125.724 MHz.
1st Stage CMFB Loop Bode Plots

Resistive feedback

Phase margin = 79.0094 Deg at frequency = 5.36771 MHz.

Capacitive feedback

Phase margin = 84.622 Deg at frequency = 6.17596 MHz.
2\textsuperscript{nd} Stage CMFB Loop Bode Plots

Resistive feedback

Phase margin = 139.738 Deg at frequency = 3.73402 MHz.

Capacitive feedback

Phase margin = 158.414 Deg at frequency = 1.51941 MHz.
Summary of pstb analysis

<table>
<thead>
<tr>
<th>Application</th>
<th>Items</th>
<th>DC Gain (dB)</th>
<th>PM (°)</th>
<th>GBW (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample hold</td>
<td>1&lt;sup&gt;st&lt;/sup&gt; stage CMFB</td>
<td>45.9</td>
<td>84.6</td>
<td>6.1</td>
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<tr>
<td></td>
<td>2&lt;sup&gt;nd&lt;/sup&gt; stage CMFB</td>
<td>1.31</td>
<td>158.4</td>
<td>1.5</td>
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<tr>
<td></td>
<td>DM loop</td>
<td>62.9</td>
<td>64.1</td>
<td>125</td>
</tr>
<tr>
<td>Resistive feedback</td>
<td>1&lt;sup&gt;st&lt;/sup&gt; stage CMFB</td>
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<td>79</td>
<td>5.3</td>
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<tr>
<td></td>
<td>2&lt;sup&gt;nd&lt;/sup&gt; stage CMFB</td>
<td>4.1</td>
<td>139.7</td>
<td>3.7</td>
</tr>
<tr>
<td></td>
<td>DM loop</td>
<td>63</td>
<td>67</td>
<td>48.6</td>
</tr>
</tbody>
</table>
Unity-gain inverting amplifier transient response with a 200mV differential step (rise/fall time=0.1ns, pulse width=200ns)
Unity-gain inverting amplifier transient response with a 100mV common mode step (rise/fall time=0.1ns, pulse width=200ns)
Sample-Hold Configuration

- Ideal switches with on resistance of 1kΩ
Sample-Hold Transient Response

- DM and CM outputs waveforms when $\text{fin}=1/4$ MHz, $\text{fs}=5$ MHz
DM and CM outputs waveforms when fin=11/4 MHz, fs=5MHz
References